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P01/7700 0.00-0318613.7

1/77

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The Patent Office

Cardiff Road
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1.	Your reference	PHGB 030134GBQ
2.	Patent application number *(The Patent Office will fill in this part)*	0318613.7 - 8 AUG 2003
3.	Full name, address and postcode of the or of each applicant (*underline all surnames*)	KONINKLIJKE PHILIPS ELECTRONICS N.V. GROENEWOUDSEWEG 1 5621 BA EINDHOVEN THE NETHERLANDS
	Patents ADP Number (*if you know it*)	07419294001
	If the applicant is a corporate body, give the country/state of its incorporation	THE NETHERLANDS
4.	Title of the invention	ELECTROLUMINESCENT DISPLAY DEVICES
5.	Name of your agent (*if you have one*)	
	"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)	Philips Intellectual Property & Standards Cross Oak Lane Redhill Surrey RH1 5HA
	Patents ADP number (*if you know it*)	08359655001

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Claims(s)	0
Abstract	0
Drawings	4

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Statement of inventorship and right to grant of a patent (*Patents Form 7/77*)

Request for preliminary examination and search (*Patents Form 9/77*)

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Any other documents (*Please specify*)

11. I/We request the grant of a patent on the basis of this application.

Signature [signature] Date 7/8/05

12. Name and daytime telephone number of person to contact in the United Kingdom 01293 81 5280 P L WILLIAMSON

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DESCRIPTION

ELECTROLUMINESCENT DISPLAY DEVICES

This invention relates to electroluminescent display devices, particularly active matrix display devices having an array of pixels comprising light-emitting electroluminescent display elements and thin film transistors. More particularly, but not exclusively, the invention is concerned with an active matrix electroluminescent display device whose pixels include light sensing elements which are responsive to light emitted by the display elements and used in the control of energisation of the display elements.

Matrix display devices employing electroluminescent, light-emitting, display elements are well known. The display elements commonly comprise organic thin film electroluminescent elements, (OLEDs), including polymer materials (PLEDs), or else light emitting diodes (LEDs). These materials typically comprise one or more layers of a semiconducting conjugated polymer sandwiched between a pair of electrodes, one of which is transparent and the other of which is of a material suitable for injecting holes or electrons into the polymer layer.

The display elements in such display devices are current driven and a conventional, analogue, drive scheme involves supplying a controllable current to the display element. Typically a current source transistor is provided as part of the pixel configuration, with the gate voltage supplied to the current source transistor determining the current through the electroluminescent (EL) display element. A storage capacitor holds the gate voltage after the addressing phase. An example of such a pixel circuit is described in EP-A-0717446.

Each pixel thus comprises the EL display element and associated driver circuitry. The driver circuitry has an address transistor which is turned on by a row address pulse on a row conductor. When the address transistor is turned on, a data voltage on a column conductor can pass to the remainder of the pixel. In particular, the address transistor supplies the column conductor

voltage to the current source, comprising the drive transistor and the storage capacitor connected to the gate of the drive transistor. The column, data, voltage is provided to the gate of the drive transistor and the gate is held at this voltage by the storage capacitor even after the row address pulse has ended. The drive transistor in this circuit is implemented as a p-channel TFT, (Thin Film Transistor) so that the storage capacitor holds the gate-source voltage fixed. This results in a fixed source-drain current through the transistor, which therefore provides the desired current source operation of the pixel. The brightness of the EL display element is approximately proportional to the current flowing through it.

In the above basic pixel circuit, differential ageing, or degradation, of the LED material, leading to a reduction in the brightness level of a pixel for a given drive current, can give rise to variations in image quality across a display. A display element that has been used extensively will be much dimmer than a display element that has been used rarely. Also, display non-uniformity problems can arise due to the variability in the characteristics of the drive transistors, particularly the threshold voltage level.

Improved voltage-addressed pixel circuits which can compensate for the ageing of the LED material and variation in transistor characteristics have been proposed. These include a light sensing element which is responsive to the light output of the display element and acts to leak stored charge on the storage capacitor in response to the light output so as to control the integrated light output of the display element during the drive period which follows the initial addressing of the pixel. Examples of this type of pixel configuration are described in detail in WO 01/20591 and EP 1 096 466. In an example embodiment, a photodiode in the pixel discharges the gate voltage stored on the storage capacitor and the EL display element ceases to emit when the gate voltage on the drive transistor reaches the threshold voltage, at which time the storage capacitor stops discharging. The rate at which charge is leaked from the photodiode is a function of the display element output, so that the photodiode serves as a light-sensitive feedback device.

With this arrangement, the light output from a display element independent of the EL display element efficiency and ageing compensation is thereby provided. Such a technique has been shown to be effective in achieving a high quality display which suffers less from non-uniformities over a period of time. However, this method requires a high instantaneous peak brightness level to achieve adequate average brightness from a pixel in a frame time and this is not beneficial to the operation of the display as the LED material is likely to age more rapidly as a result.

There have been refinements, proposed to this kind of voltage addressed pixel circuit, for example as described in British Patent Application No 0305632.2 (PHGB 030025) to correct as well for the effects of stress induced threshold voltage variations in the drive transistors which supply current to the EL elements of the pixels, allowing the possibility of amorphous silicon TFTs to be used for the drive transistors.

A problem with these pixel circuits is that they add increasing complexity to the pixel circuit and require more components for the pixel circuit which makes high resolution display more difficult to fabricate.

It is an object of the present invention to provide an improved active matrix electroluminescent display device of the kind in which pixels include a photosensitive device, such as a photodiode, in the pixel that is responsive to light produced by the EL display element of the pixel.

The present invention provides an active matrix electroluminescent display device which overcomes to an extent at least the problem found with the known display devices.

According to an aspect of the present invention, a pixel circuit is simplified by transferring at least some of the complexity of the pixel circuit to the drive circuit for the array of pixels, so that the pixel circuit comprises substantially only those elements essential to its operation. In this way more complex circuits are accommodated in the drive circuit, preferably the column drive circuit, and not in the pixels themselves.

Various novel concepts, arrangements and features, inventive concepts, arrangements and features, and specific embodiments are disclosed

herein, particularly but not exclusively with reference to the accompanying drawing Figures.

In a preferred embodiment of the present invention, a pixel circuit includes an EL display element, a current source (drive transistor), a memory element, and a switch allowing the pixel to be addressed with a data signal, these components providing a conventional, basic, active matrix pixel circuit and the minimum required for active matrix operation. The circuit then may further include a photosensitive device, for example a photodiode or phototransistor, an associated memory element and a further switch. The photosensitive element senses the brightness of the EL display element which is converted to an electrical charge indicative of the brightness level and stored in the pixel, by means of the associated memory element, for example a capacitor. This charge can be read-out from the pixel at some subsequent time, enabling the brightness of the pixel for a given data signal voltage level to be determined. This information can then be used to adjust the input data signal voltages supplied to each pixel so as to correct for varying TFT threshold voltage and mobility and the EL display element efficiency. This correction can be performed in the drive circuit outside the pixel array, preferably within the column drive circuitry supplying the data signals to the pixels.

In another preferred embodiment, each pixel additionally includes another switch for controlling the energisability of the display element, and involves sharing of addressing (selection) and data signal lines with a view to maximizing pixel apertures.

Advantageous features in accordance with the present invention are illustrated specifically in embodiments of various aspects of the present invention now to be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a simplified schematic diagram of an embodiment of active matrix EL display device;

Figure 2 illustrates a known form of pixel circuit;

Figures 3, 4 and 5 illustrate schematically pixel circuits in embodiments of display device according to the present invention; and

Figure 6 shows schematically circuitry external to a pixel for adjusting data supplied to the pixel in an embodiment of display device according to the present invention.

The same reference numbers are used throughout the Figures to denote the same or similar parts.

Referring to Figure 1, the active matrix EL display device comprises a panel having a row and column matrix array of regularly – spaced pixels, denoted by the blocks 10, each comprising an EL display element 20 and an associated driving circuit controlling the current through the display element. The pixels are located at the intersections between crossing sets of row (selection) and column (data) address conductors, or lines, 12 and 14. Only a few pixels are shown here for simplicity. The pixels 10 are addressed via the sets of address conductors by a peripheral drive circuit comprising a row, scanning, driver circuit 16 and a column, data, driver circuit 18 connected to the ends of the respective conductor sets.

Each row of pixels is addressed in turn in a frame period by means of a selection pulse signal applied by the circuit 16 to the relevant row conductor 12 so as to program the pixels of the row with respective data signals which determine their individual display outputs in a frame period that follows the address period, the data signals being supplied in parallel by the circuit 18 to the column conductors 14. As each row is addressed, the data signals are supplied by the circuit 18 in appropriate synchronisation.

The EL display element 20 of each pixel comprises an organic light emitting diode, represented here as a diode element (LED), and comprising a pair of electrodes between which one or more active layers of organic electroluminescent light-emitting material are sandwiched. In this particular embodiment the material comprises a polymer LED material, although other organic electroluminescent materials, such as low molecular weight materials, could be used. The display elements of the array are carried, together with their associated active matrix circuitry, on the surface of an insulating

substrate. The substrate is of transparent material, for example glass, and either the cathodes or anodes of the display elements 20 are formed of a transparent conductive material, such as ITO, so that light generated by the electroluminescent layer is transmitted through these electrodes. Typical examples of suitable organic conjugated polymer materials which can be used for the EL material are described in WO 96/36959. Typical examples of other, low molecular weight, organic materials are described in EP-A-0717446.

The driving circuit of each pixel 10 includes a drive transistor, comprising a low temperature polysilicon TFT (thin film transistor), which is responsible for controlling the current through the display element 20 on the basis of a data signal voltage applied to the pixel via a column conductor 14 which is shared by a respective column of pixels. The column conductor 14 is coupled to the gate of the current-controlling drive TFT through an address TFT in the pixel driving circuit and the gates for the address TFTs of a row pixels are all connected to a respective, common, row address conductor 12.

Although not shown in Figure 1, each row of pixels 10 also shares, in conventional manner, a respective power supply line held at a predetermined voltage, and a reference potential line, usually provided as a continuous electrode common to all pixels. The display element 20 and the drive TFT are connected in series between the power supply line and the common reference potential line. The reference potential line, for example, may be at ground potential and the power supply line at a positive potential around, for example, 12V with respect thereto.

The features of the display device described thus far are generally similar to those of known devices.

Figure 2 illustrates a known form of pixel circuit, as described in WO 01/20591 for example. Here the drive TFT and the address TFT, both comprising p-channel devices, are referenced at 22 and 26 respectively, and the power supply line and reference potential line are referenced at 32 and 30 respectively. When the address TFT 26 is turned on in a respective row address period by a selection pulse signal applied to the row conductor 12, a voltage (data signal) on the column conductor 14 can pass to the remainder of

the pixel. In particular, the TFT 26 supplies the column conductor voltage to a current source circuit 25 comprising the drive TFT 22 and a storage capacitor 24 connected between the gate of the TFT 22 and the power supply line 32. Thus, the column voltage is provided to the gate of the TFT 22 which is held at this voltage, constituting a stored control value, by the storage capacitor 24 even after the address TFT 26 is turned off at the end of the row address period. The drive TFT 22 is here implemented as a P-channel TFT and the capacitor 24 holds the gate – source voltage. This results in a fixed source – drain current through the TFT 22, which therefore provides the desired current source operation of the pixel. Electrical current through the display element 20 is regulated by the drive TFT 22 and is a function of the gate voltage on the TFT 22, which is dependent upon the stored control value determined by the column voltage, data, signal. At the end of the row address period, the voltage retained by the storage capacitor 24 maintains the operation of the display element during the subsequent drive period before the pixel is addressed again in the next frame period. The voltage between the gate of the TFT 22 and the reference potential line 32 thus determines the current passing through the display element 20, and in turn controls the instantaneous light output level of the pixel.

The known pixel circuit of Figure 2 further includes a discharge photodiode 34, which is reverse biased and responsive to light emitted by the display element 20 and acts to decay the charge stored on the storage capacitor 24 in dependence on light emitted by the element 20, via the photocurrent generated in the photodiode. The photodiode discharges the gate voltage stored on the capacitor 24 and when the gate voltage on the TFT 22 reaches the TFT's threshold voltage the display element 20 will no longer emit light and the storage capacitor stops discharging. The rate at which charge is leaked from the photodiode 34 is a function of the display element light output level so that the photodiode 34 functions as a light sensitive feedback device.

The photodiode feedback arrangement is used to compensate for the degradational effects of display element ageing, whereby the efficiency of its

operation in terms of the light output level produced for a given drive current diminishes. Through such degradation display elements that have been driven longer and harder will exhibit reduced brightness, causing display non-uniformities. The photodiode arrangement counteracts these effects by appropriately controlling the integrated, total, light output from a display element in the drive period, corresponding to a frame period at maximum. The length of time for which a display element is energized to generate light during the drive period which follows the address period is regulated according to the existing drive current light emission level characteristic of the display element, as well as the level of the applied data signal, such that the effects of degradation are reduced. Degraded, dimmer, display elements will result in the pixel driving circuit energizing the display element for a period longer than that for an un-degraded, brighter, display element so that the average brightness can remain the same over an extended period of time of device operation.

The average light output in the drive period is dependent on the efficiency of the photodiode 34, which is highly uniform across the array of pixels, and is independent of the efficiency of the LED element. However, the output is dependent also on the threshold voltage of the drive TFT 22 and as this can vary from pixel to pixel display non-uniformity may occur. The pixel circuit of Figure 2 also requires an efficient photodiode, typically an amorphous silicon pin photodiode and relatively high peak brightness to achieve reasonable average brightness. The decay of the charge stored on the storage capacitor 24 means also that the circuit operates at comparatively low brightness levels for most of the drive period. The circuit thus operates the LED at low efficiency and, therefore, can lead to increased ageing.

Figure 3 illustrates an embodiment of pixel circuit 10 in a display device according to the present invention, and more particularly shows the basic principle of an external optical feedback approach used in the display device. In this pixel circuit a photosensitive device, here in the form of a photodiode 40, is again used to sense in the pixel light output from the display element 20. A storage capacitor 44, separate from the data signal storage capacitor 24, is

connected across the photodiode 40 and accumulates charge produced as a result of light from the display element 20 falling on the photodiode 40. This storage capacitor 44 could perhaps be the intrinsic self-capacitance of the photodiode rather than a separate component. The amount of charge stored on the capacitor 24 is determined by the brightness of the pixel and varies accordingly.

The photodiode 40 is connected at its one side to a voltage supply, here the power line 32, and at its other side to a sense column line 46 via a switching TFT 45 whose operation is controlled by a control signal on a read out control line 48. This line 48 is shared by all pixels in the same row such that the switches 45 of all pixels in the row are operated simultaneously, while the sense line 46 is shared by all pixels in the same column. The charge accumulated by the capacitor 44 is read out through the line 46 upon operation of the switch 45 to a circuit outside the pixel array where it is measured and used in determining adjustments to data signals supplied to the pixels. It will be appreciated, therefore, that unlike the circuit of Figure 2 the light output sensing part of the pixel circuit is not directly associated with the current source part of the circuit.

The pixel further includes an isolating TFT 36 connected between the drive TFT 22 and the display element 20 which can be opened, so as to isolate the display element 20 from the drive TFT 22, or closed, so as to allow the drive TFT to drive the display element and produce light output, by means of switching signals on the control line 48 connected to its gate, and shared by other pixels in the same row. The switch 45 enables the display element 20 to be maintained off during addressing of the pixel with a data signal so that no light is produced during this addressing period and no current is, therefore, drawn through the power line 32. This avoids the possibility of voltage drops occurring along the line 32, and consequential crosstalk.

In a preferred mode of operation, with the display element 20 being energized by current supplied by the TFT 22 to generate light output, the photodiode 40 is isolated from the sense line 46, by maintaining the switching TFT 45 open, so as to allow charge resulting from illumination of the

photodiode 40, to accumulate on the capacitor 44. In this way, a useful charge signal can be accumulated to make read-out simpler. Charge read-out, via the sense line 46, upon closing of the switching TFT 45, is preferable to current, or voltage, forms of signal read out as the sensitivity of an amplifier circuit connected to the line 46 for providing an indication of the level of the signal can be much greater and the dynamic range possible considerably larger.

In order to provide an indication of the threshold voltage level and mobility of the drive TFTs 22 of pixels in the array, the display device may be driven so as to produce a series (at least two) of plain field images at different brightness levels. The signals stored on the photodiode storage capacitors 44 of the pixels for each plain field image would then be read out, by operating the switches 45, via the sense lines 46. Such read out would be for a row of pixels at a time, with the stored charges being read out for each row in sequence following one of the plain image fields, and then again following the next plain image field. From the data thereby obtained from each pixel, the mobility and the threshold voltage of the drive TFTs 22 of the pixel away can be calculated. As these values do not vary significantly over time in the case of the drive TFTs 22 comprising polycrystalline silicon type TFTs, this operation would only need to be performed very occasionally or possibly only at the time of manufacturing the device. At suitable intervals over the life of the display device, for example each time the device is turned on, the device may be arranged to be operated with a threshold/mobility corrected plain field image and the sensed charge again read out. Any irregularities in the display image would then likely be due simply to the ageing effects of the EL material of the display elements and could be cancelled by appropriate image data correction. In the case of the drive TFTs 22 comprising amorphous silicon TFTs, whose characteristics may vary as a result of the level of driving of individual pixels over the device's lifetime, then such read out procedures preferably are performed more frequently.

Figure 4 shows schematically a preferred implementation of the pixel circuit of Figure 3. Here, the same column line, 14/46, is used both for the supply of data signals and read out of charge signals from a pixel. Also, the

same row address line is used for both the switching TFTs 45 and 36 of the pixels in a row.

Figure 5 illustrates a modified form of the pixel circuit of Figure 3, in which a phototransistor 50 is used as a photosensitive device rather than the photodiode 40, the gate of the phototransistor 50 being coupled to the anode of the display element 20. The switches 45 are of opposite conductivity (p type) to the switches 36 (n type).

An example operating scheme for the above described pixel circuit of Figure 5 will now be described. The display device is first operated by addressing the rows of pixels a row at a time, as usual, with appropriate data signals to produce a uniform grey level image from the pixels, with the switch TFTs 36 being turned off during addressing and then turned on in the subsequent display phase to allow energisation of the display elements and light emission. The switches 36 are then operated, via their switch control lines 37, so as to open, row by row. This has the effect of extinguishing each row of pixels in turn. At the same time as the switching of the switches 37 of each row, the switching TFTs 45 are operated, in complementary fashion, so as to connect the capacitors 44 of a row of pixels at a time to the shared column line 14/46. The stored charge can then be reset in preparation for a sensing procedure. This gives a clear start point for a sense operation. As each row ceases to be addressed, the EL display elements of the row of pixels are re-illuminated and charge integration in the storage capacitors 44 of those pixels would begins. At the end of a predetermined illumination period, the display device is addressed, a row at a time, to turn off the display elements. In this way the end of charge integration can be set accurately without disturbing the stored charge. This charge may then be read out slowly in a following period.

It is possible to operate the display device and pixels in other ways to achieve the same function, and also to use alternative pixel circuit designs.

The above described pixel circuits are intended to use polycrystalline silicon TFTs. Other variants suitable for using amorphous silicon TFTs are possible. In this case the sense read out scheme would be usable also to

compensate for threshold voltage drift in the drive TFTs as well as LED material degradation.

Figure 6 shows a pixel circuit variant suitable for use with amorphous silicon technology. The switch line 37 controls the switch 36 which is here connected in parallel with the drive TFT 22 of the pixel rather than in series. Closure of the switch 36 pulls the anode of the display element 20 high, to the voltage of the power line 32, for the addressing phase so that the correct data voltage will be programmed across the drive TFT 22. The phototransistor 50 can be biased by connecting its gate to a suitable node in the pixel circuit, or possibly a pixel in the previous row, depending on the drive scheme used. The pixel then operates in similar manner to the previous embodiments. In this case, though, the display device is not corrected simply at the manufacturing stage, but periodically during use. the correction obtained should now be for both threshold voltage drift and LED material degradation.

Figure 7 illustrates schematically circuitry external to the pixels for performing the necessary corrections, and obtaining adjusted data signals for supply to the pixels, in a display device using any of the pixel circuit embodiments of Figures 3, 4, 5 and 6, this circuitry preferably, and conveniently, being incorporated in the column driver circuit 18.

When the display device is in its sense mode, with charge being read out via the sense line 46 or combined sense and data line 14/46, the charge for one pixel is measured using a charge sensitive amplifier 70. The output of the amplifier is supplied to an analogue to digital converter 72 and the resulting digital data indicative of the level of charge read out is stored in a corresponding look up table (LUT) 74, 76. During display device programming data relating to the threshold voltage and mobility of the drive TFTs 22 and the LED material degradation from respective stores 80 and 82 associated with the LUTs 74 and 76 are combined at 84 and added, at adder 88, to the pixel data, which is obtained in the column driver circuit 18 and supplied to an input 86 of this correction circuitry. The appropriately corrected data signal then output by the adder 88 is supplied, via a digital to analogue convertor 90 and buffer 9, to the data signal line 14 for supply to a pixel.

The read out of charge from the column line 14/46 and supply of data signals thereto is controlled by switches 92 and 94 which are operated alternately.

Each column of pixels is associated with a similar correction circuit.

In the case of an amorphous silicon TFT pixel circuit, there would only be one set of data, which contains offsets for both the threshold voltage and the LED material degradation.

Although examples of circuits using polycrystalline and amorphous silicon TFTs, microcrystalline silicon TFTs may also be used.

The photodiodes 40 are preferably pin devices.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of active matrix EL display devices and component parts therefor and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

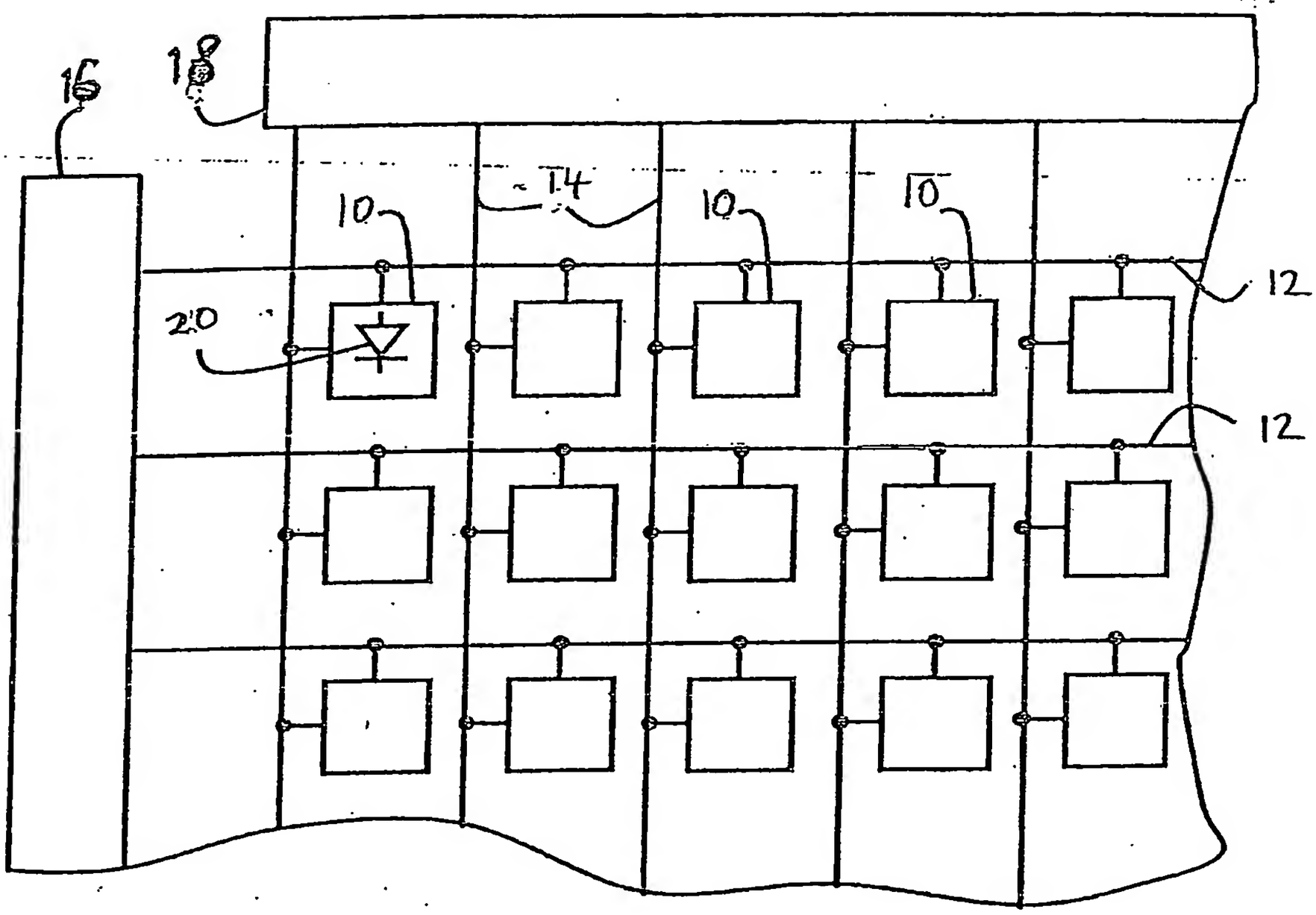


FIG. 1

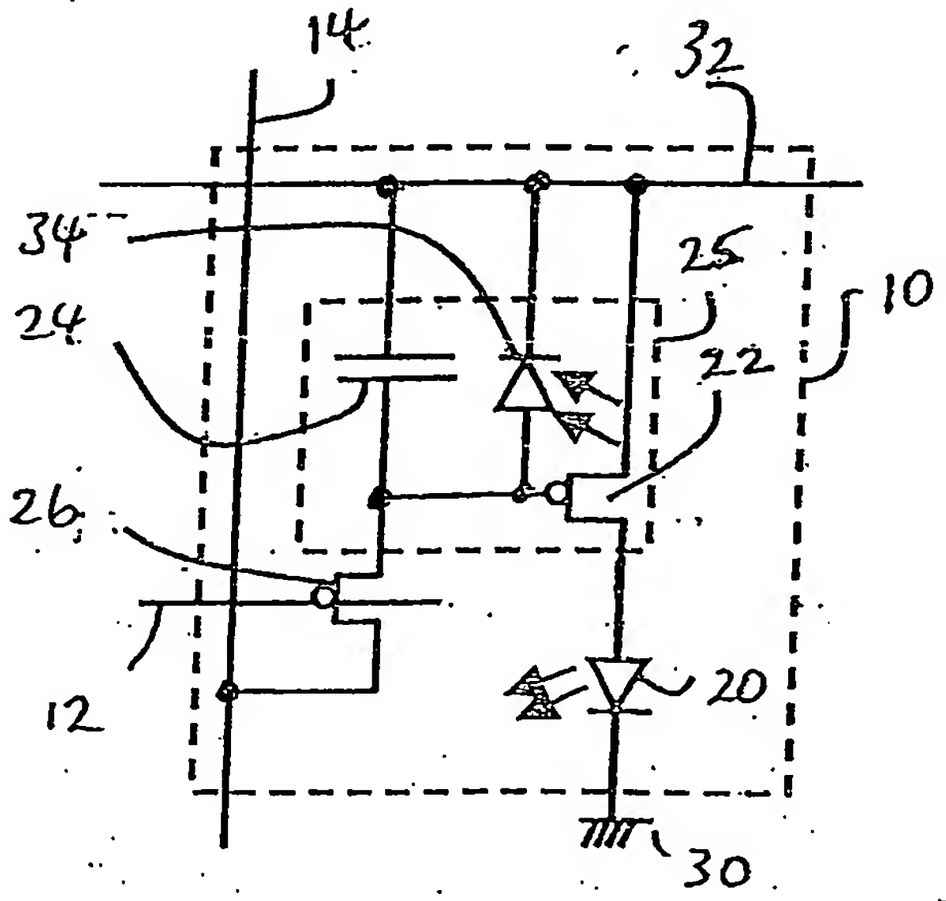
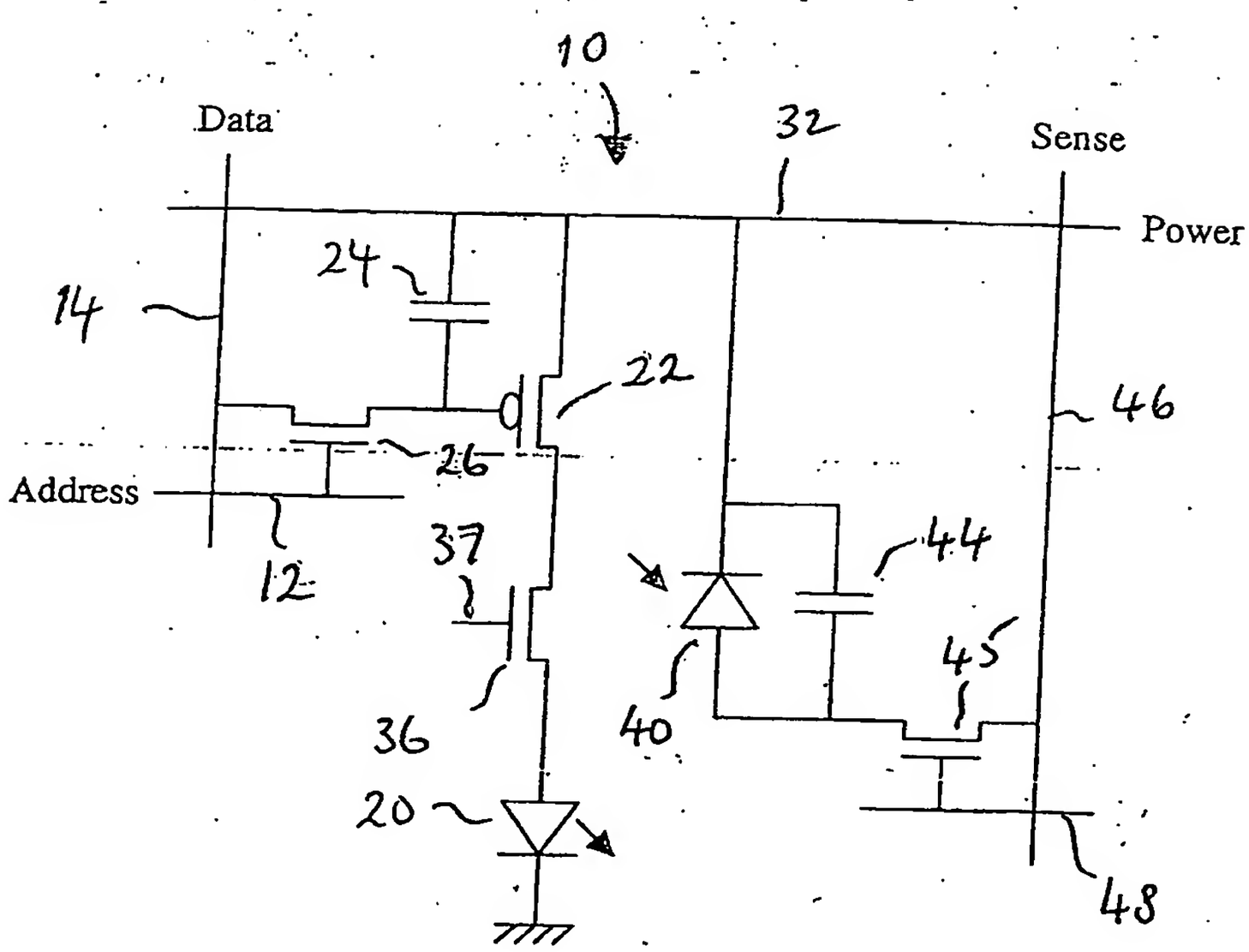


FIG. 2


214
10
Data
32
Sense
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46
26
Address
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44
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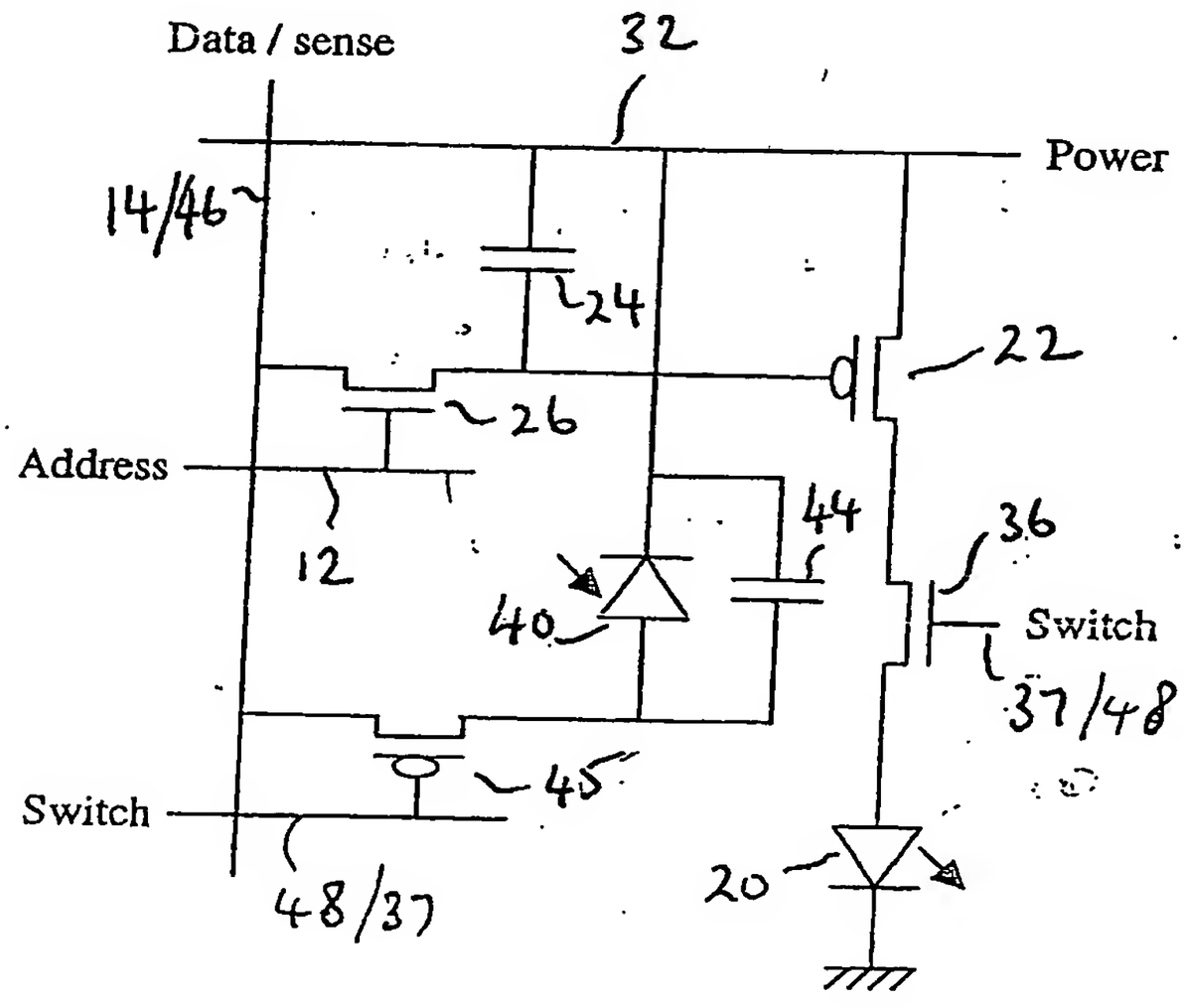
20
48

FIG.3.


Data / sense
32
Power
14/46
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22
26
Address
12
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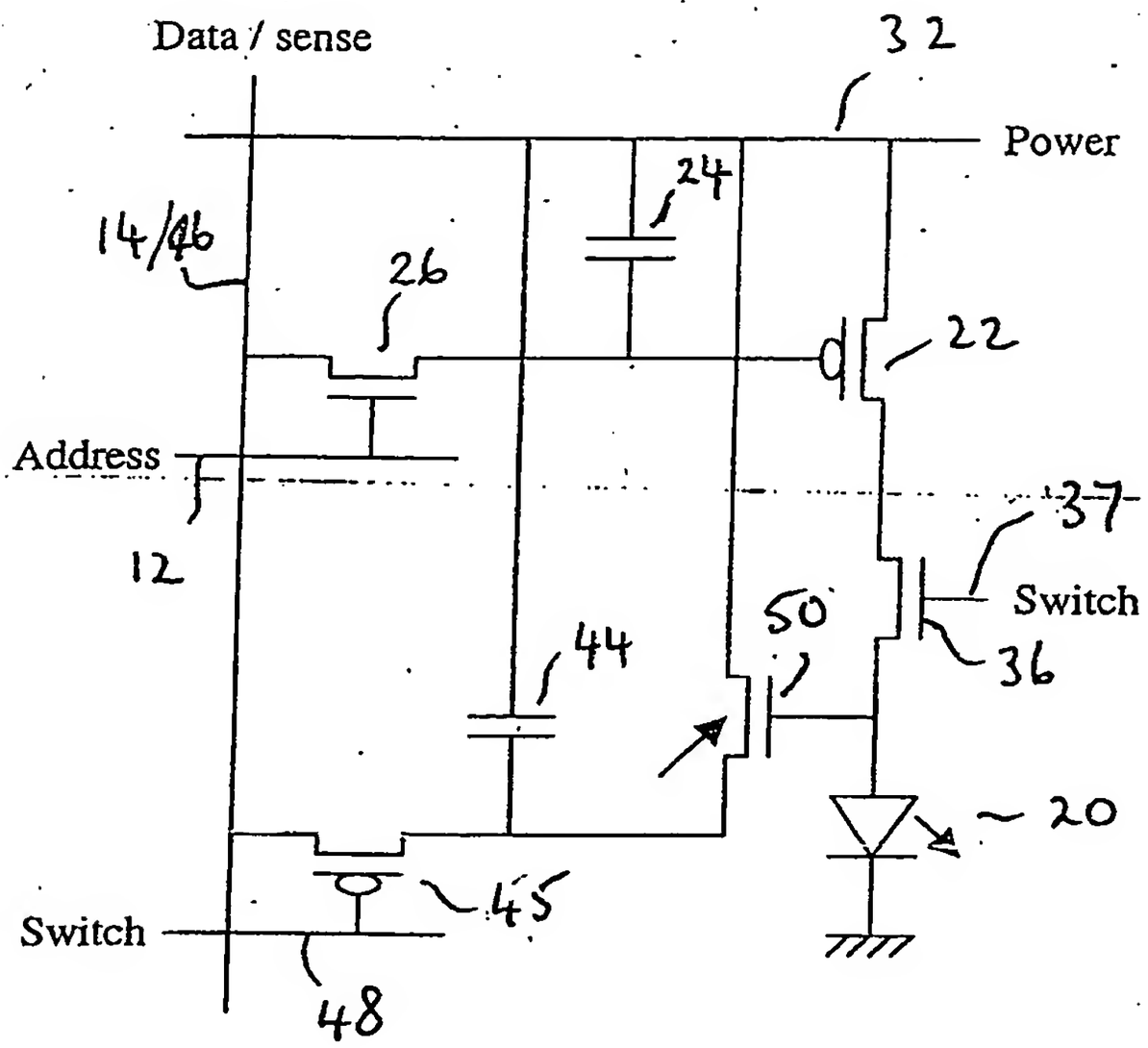
36
40
Switch
37/48
45
Switch
48/37
20

FIG. 4.


Data / sense
32
Power
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14/46
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22
Address
12
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Switch
36
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44
20
45
Switch
48

FIG. 5.

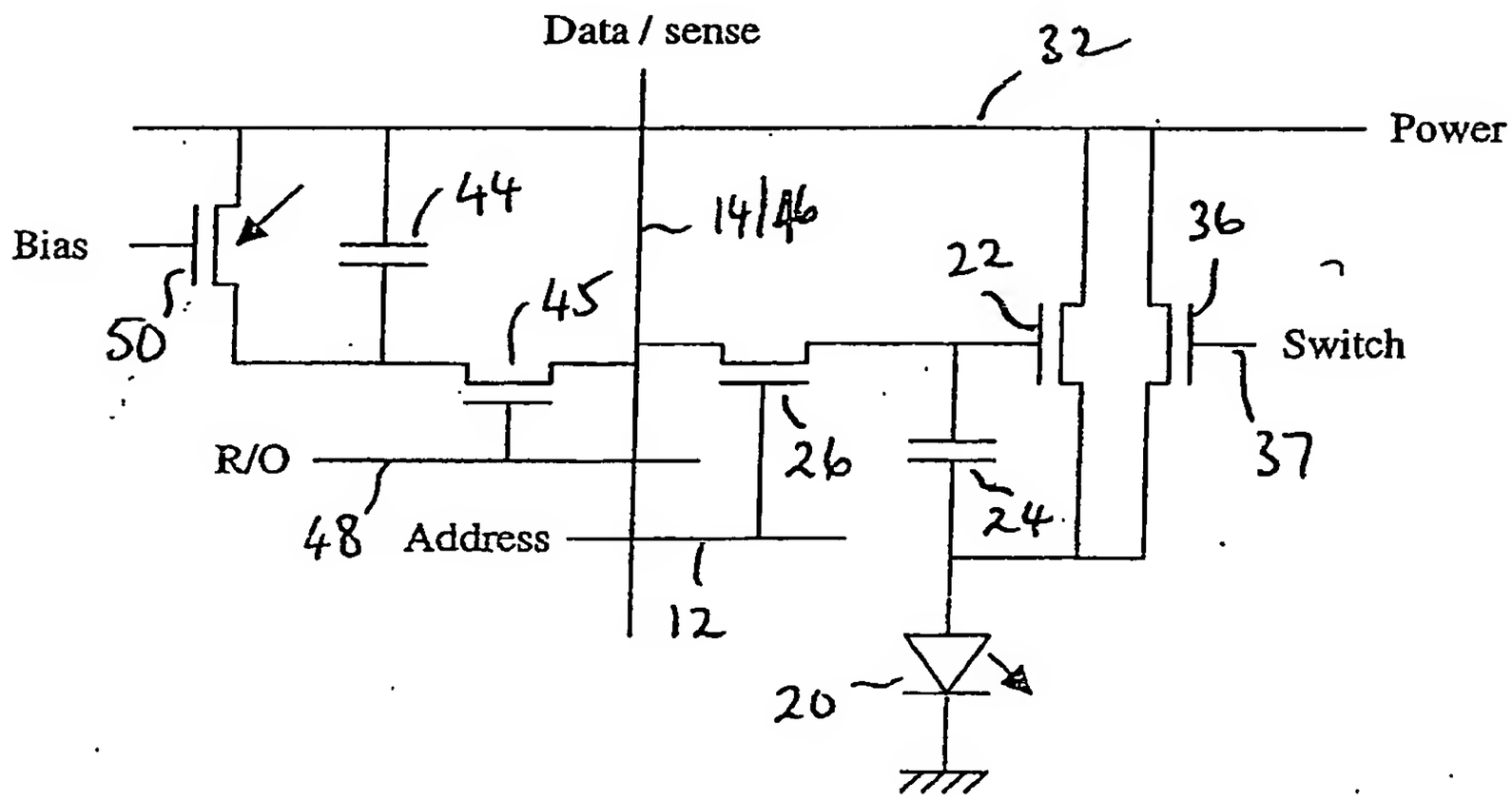
Data / sense
32
Power
Bias
44
14/46
36
22
50
45
Switch
R/O
26
37
24
48
Address
12
20

FIG. 6.

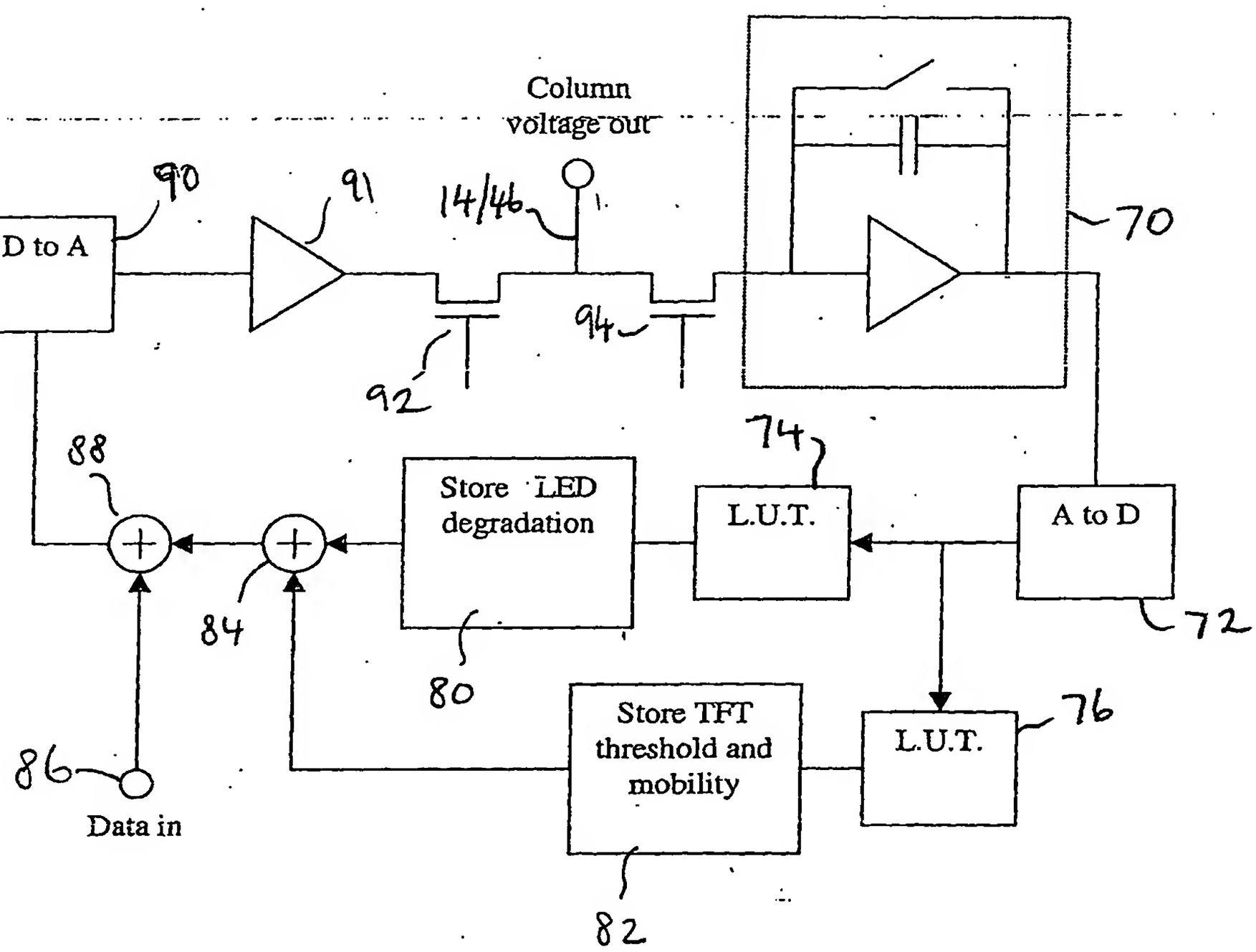
Column voltage out
90
91
14/46
70
D to A
94
92
74
88
Store LED degradation
L.U.T.
A to D
84
72
80
Store TFT threshold and mobility
L.U.T.
76
86
Data in
82

FIG. 7.